

Coldfire ASD_APS Board Support Package[†]

Version 0.1

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Abstract

Description of the `asd_aps` board and its associated board support package.

1 Introduction

The `asd_aps` board was originally developed for the AFCO Systems Development Advanced Power Strip. It is built around a Coldfire MC5485 processor. The main components of the board are:

- 128 MB DDR2 RAM attached to the SDRAM controller port.
- 8 MB flash device (boot flash) enabled by Flexbus CS0.
- 32 MB flash device (code flash) enabled by Flexbus CS1.
- A custom CPLD device having a 64 Kbyte addressable window, enabled by Flexbus CS2. This is loaded from a separate on-board EEPROM at powerup.
- An optional LCD device. This device has a 1Mbyte addressable window, and is enabled by Flexbus CS5.

1.1 Power-On Memory Map

When the system reaches its stable configuration, the resulting memory map looks like:

Base	Bound	Item	Notes
0x00000000	0xFFFFFFFF	Boot Flash	
0x80000000	0x8003FFFF	MBAR Region	

The decode logic causes any address within the MBAR region to be resolved to the on-CPU register. That is: MBAR sits “in front of” the other memory.

If you look below, you will see that boot flash will not be moving. This is in contrast to the behavior of the default bootstrap on the board.

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1.2 Evaluation Board Memory Map

The evaluation board normally organizes its memory as follows:

Base	Bound	Item	Notes
0x00000000	0x003FFFFFF	SDRAM	4M
0x00400000	0x00FFFFFF	SDRAM	Additional 12M (optional)
0x10000000	0x1003FFFF	MBAR	
0x20000000	0x20000FFF	SRAM0	
0x20001000	0x20001FFF	SRAM1	
0xe0000000	0xe1000000	Code Flash	16 Mbyte
0xff800000	0xff9FFFFFF	Boot Flash	2 Mbyte

The boot flash is "migrated" by exploiting a sleazy trick. Code in the boot flash is compiled with a base address of 0xff800000. The first 1024 bytes form the exception vector, and the word at byte 4 is the initial PC. At power-on, the ROM is set up to chip select at address zero. The code nonetheless runs from the high address because the upper bits of the physical address are not decoded by the FLASH device (i.e. the flash is aliased at the external bus layer). Eventually the COLILO bootstrap code reprograms the flexbus CS0 chip select register for a base address of 0xff800000, but this does not have any impact on the running code.

1.3 Coyotos Memory Map

When the system reaches its stable configuration, the resulting memory map looks like:

Base	Bound	Item	Notes
0x00000000	0x007FFFFFF	Boot Flash	
0x10000000	0x11FFFFFF	Code Flash	
0xC0000000	0xC7FFFFFF	SDRAM	ACR0, ACR2 used to direct map this for supervisor-only access.
0xD0000000	0xD00FFFFFF	Device Registers	1 Mbyte non-cacheable region used for device registers. ACR3 used to set cacheability attributes.
0xD0000000	0xD003FFFF	MBAR Region	256 Kbyte MBAR register region.
0xD0040000	0xD004FFFF	MMUBAR Region	64 Kbyte MMU memory map.
0xD0100000	0xD0100FFF	SRAM0	
0xD0101000	0xD0101FFF	SRAM1	
0xD0110000	0xD011FFFF	CPLD SRAM	Window into on-CPLD SRAM
0xD1000000	0xD10FFFFFF	LCD Display	Display bitmap
0xF0000000	0xFFFFFFFF	<i>Kernel</i>	Used for transient mappings, etc.